When Does Moore's Law Get Us to One Billion Transistors?

John H. Crawford
Intel Fellow
Enterprise Platform Group
Intel Corporation

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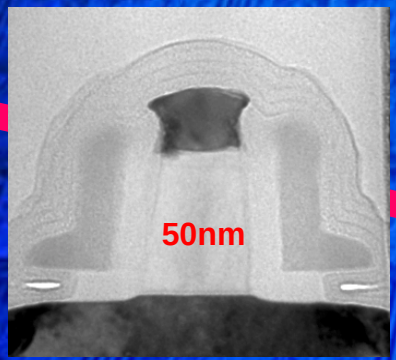
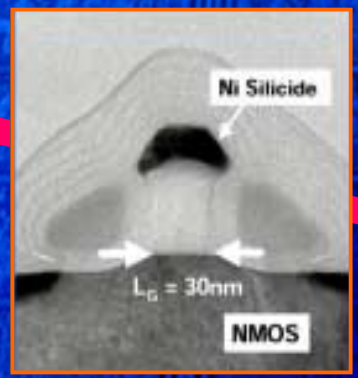
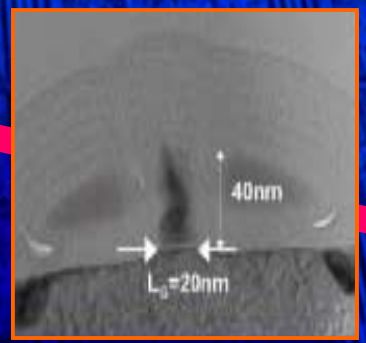
Nanotechnology Advancements



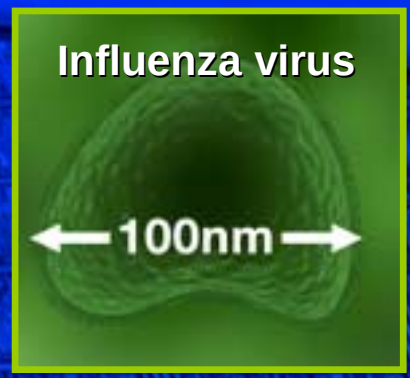
90nm Node
Lgate = 50nm
Production - 2003

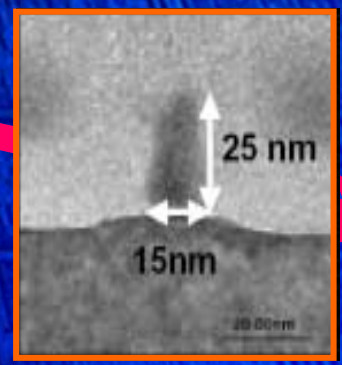


65nm Node
Lgate = 30nm
Production - 2005



45nm Node
Lgate = 20nm
Production - 2007



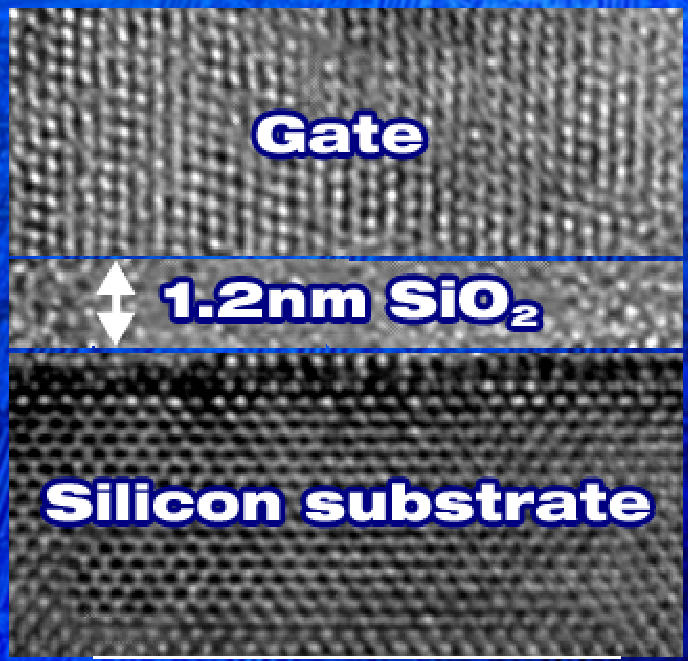


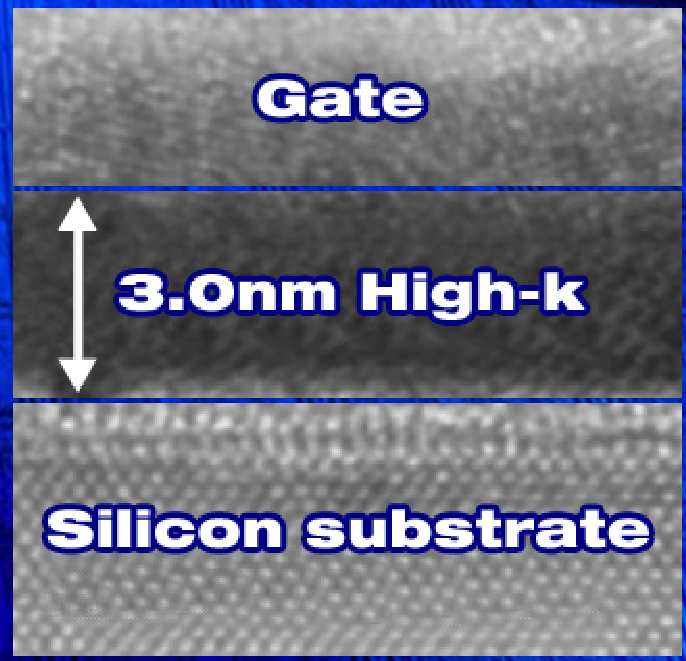
30nm Node
Lgate = 15nm
Production - 2009

Process Advancements Fulfill Moore's Law

Source: Intel

Nanotechnology Gate Dielectrics



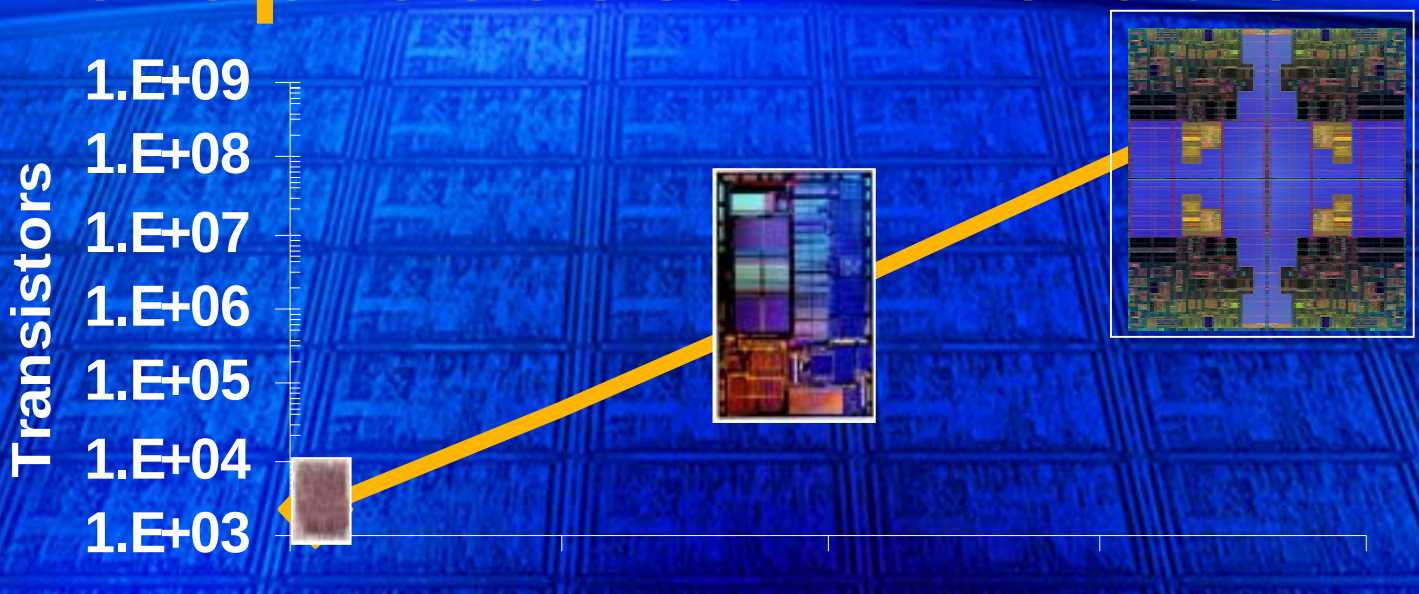


Source: Intel

	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

New Materials Support Continued Scaling

Microprocessor Evolution



	4004	Intel® 486 processor	Future processor
Date	1971	1989 (18 yrs)	2007 (+18 yrs)
Transistor Count	2300 transistors	1.2M (500 X)	1000M (800 X)
Mfg. Process	10um process	1.0 um (1/10 X)	65nm (1/15 X)
Wafer Area	50mm wafer	100-150mm (4-9X area)	300mm (4-9 X area)
Die Size	12mm2	174mm2 (14 X)	400mm^2 (2.3 X)
Core Frequency	108 kHz	25 MHz (250 X)	6 GHz (240 X)

Moore's Law delivers 1 Billion Transistors circa 2007

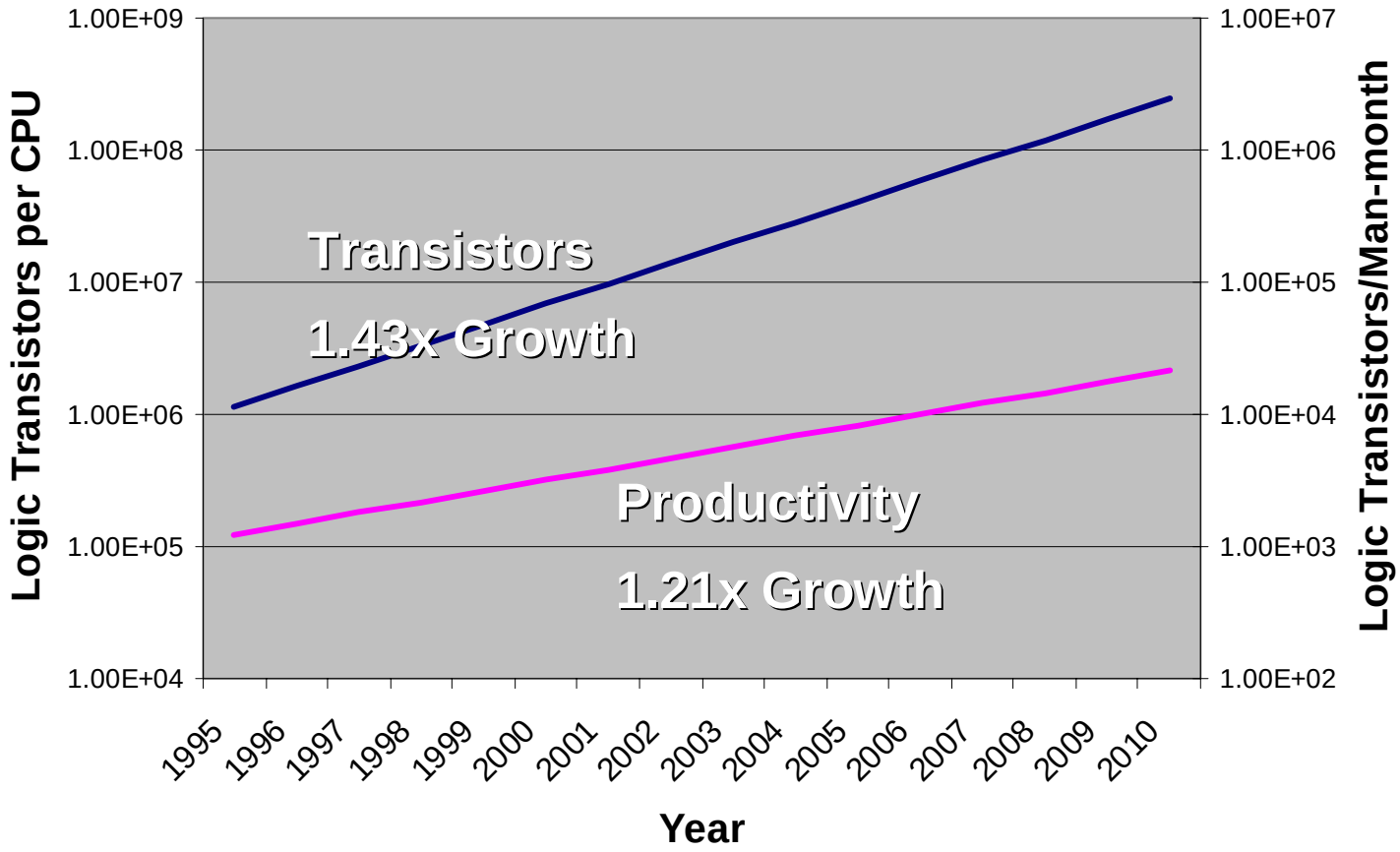
"If the automobile industry advanced as rapidly as the semiconductor industry, a Rolls Royce would get a million miles per gallon and it would be cheaper to throw it away than to park it."

Gordon Moore,
Intel Corporation

Design Challenges

- Wafer Fabrication Factory Cost
  - Increases over time
  - Now >$2B
- Visibility Inside the Chip for Test & Debug
  - Pin Bandwidth/Transistor continues to decline
  - Shrinking dimensions, increasing speeds, …
- Design Complexity
  - Productivity Tools and Methods Advance
    …But at slower rate than Moore's Law
- Power
  - Power Delivery – di/dt of Amps/nano-second
  - Thermals: Overall power and thermal density

Design Productivity Improvements

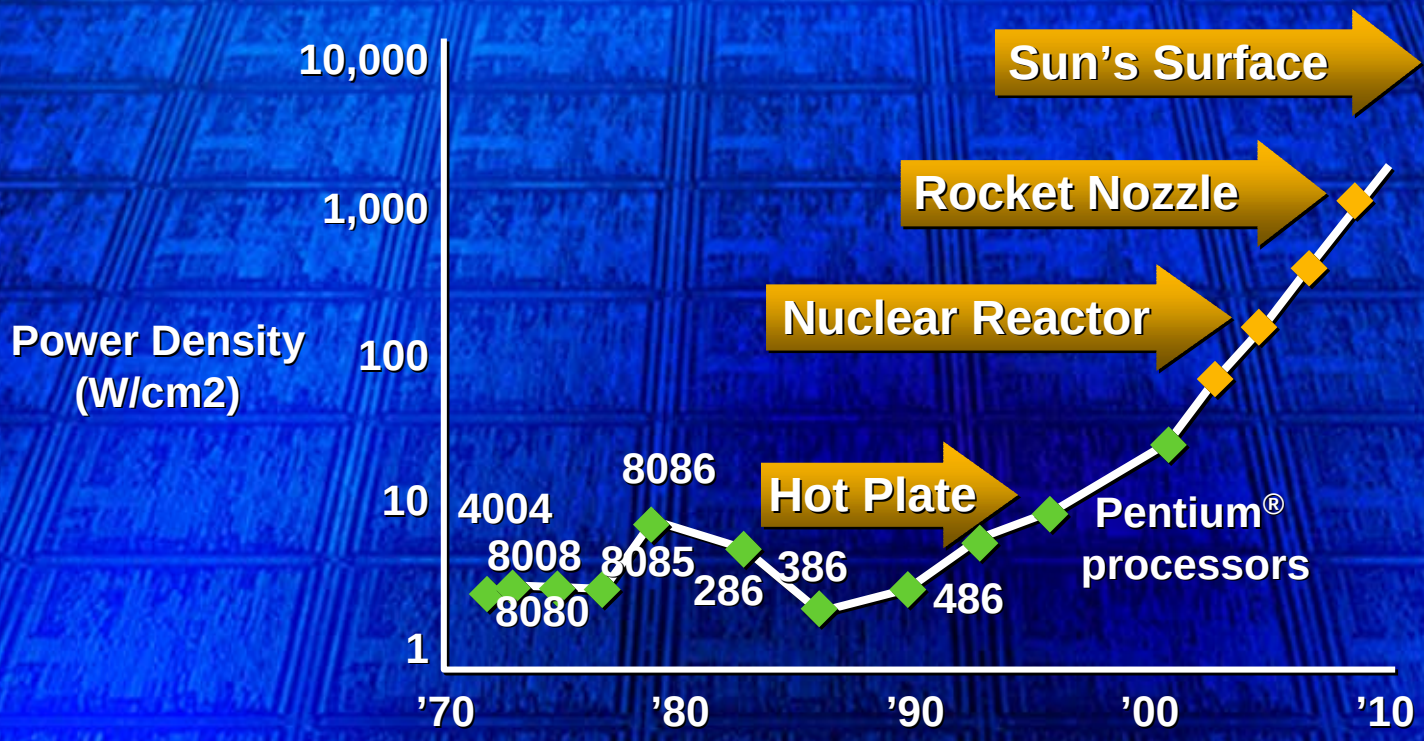


Productivity Tools and Methods Advance

…But at slower rate than Moore's Law

Eric Kronstadt, HPCA 2003

Power Density Will Get Even Worse

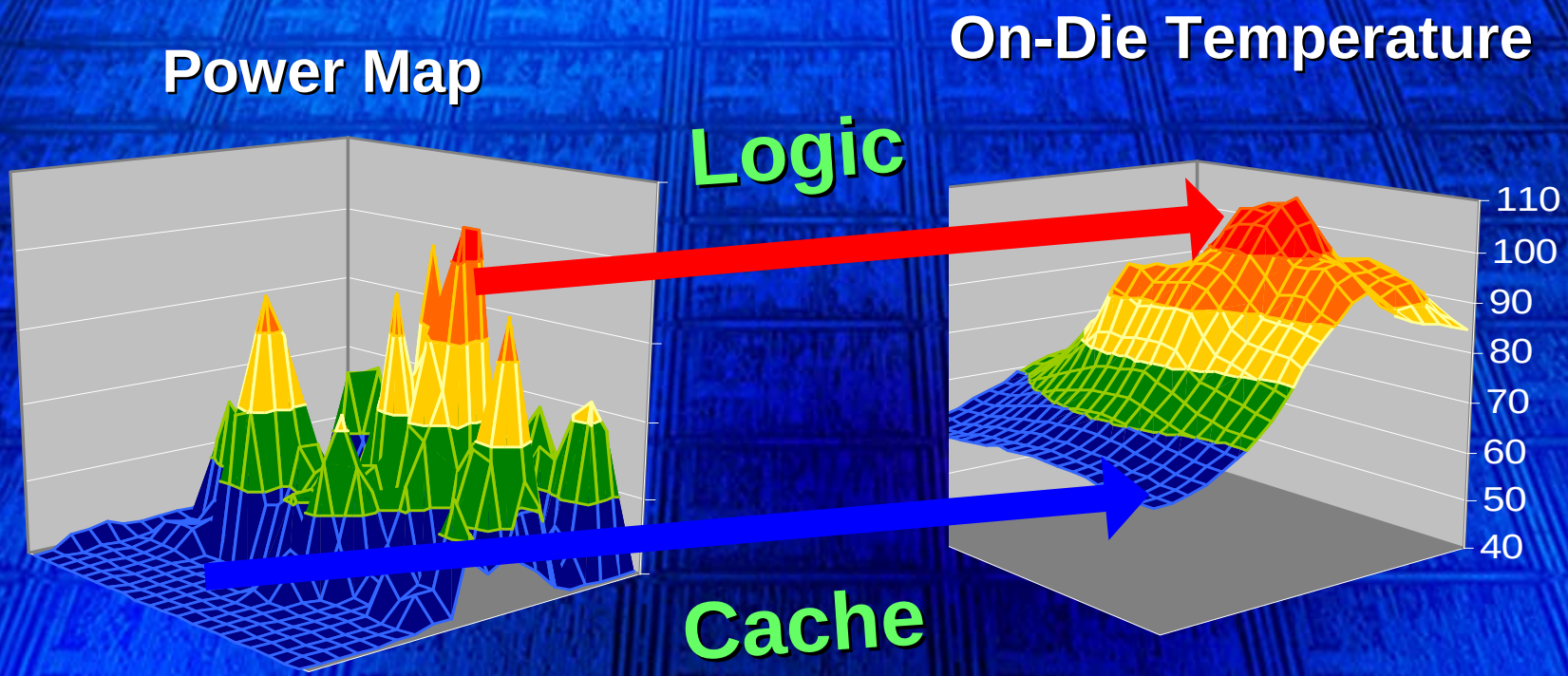


Need to Keep the Junctions Cool

- Performance (Higher Frequency)
- Lower leakage (Exponential)
- Better reliability (Exponential)

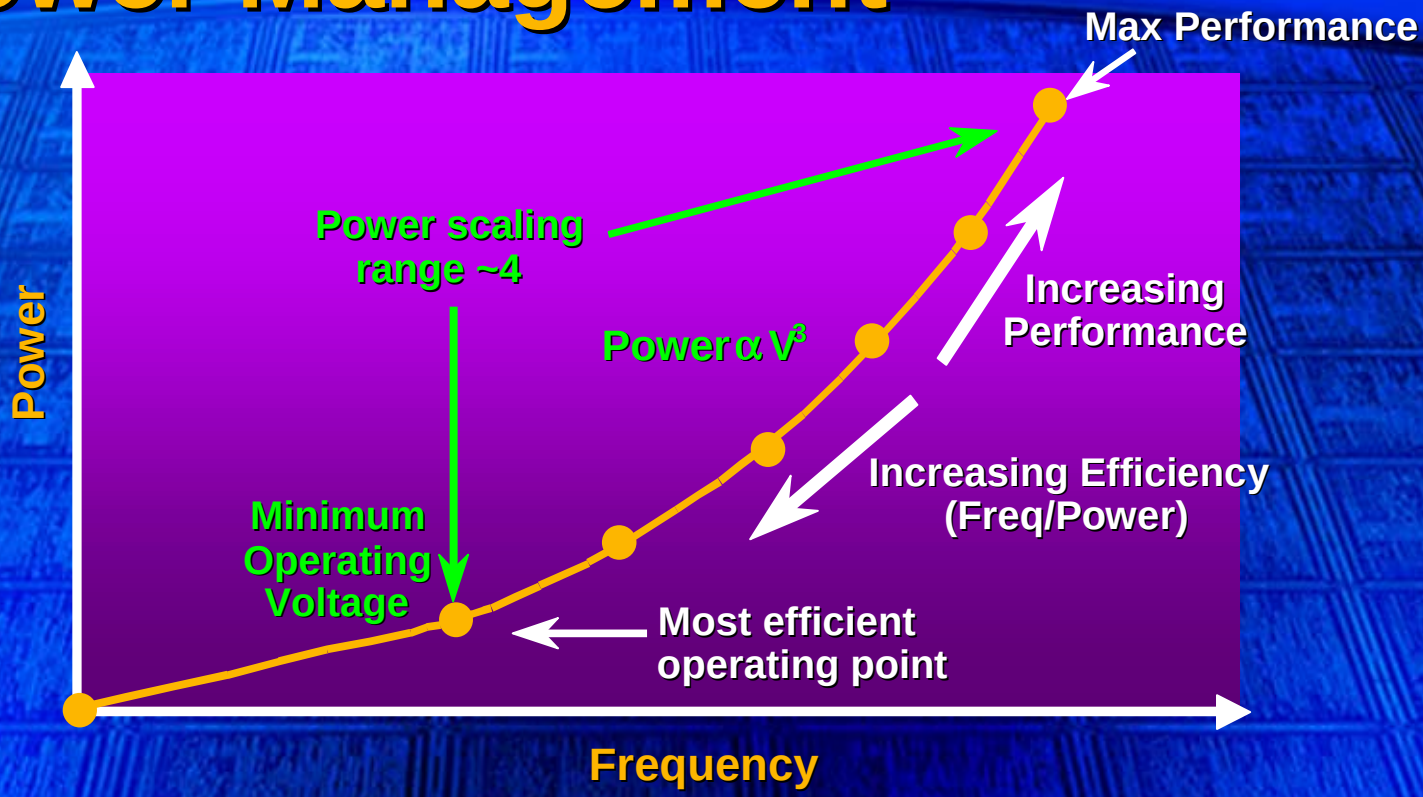
Pat Gelsinger, ISSCC 2001

Power Density



Logic runs hot - Cache runs cool

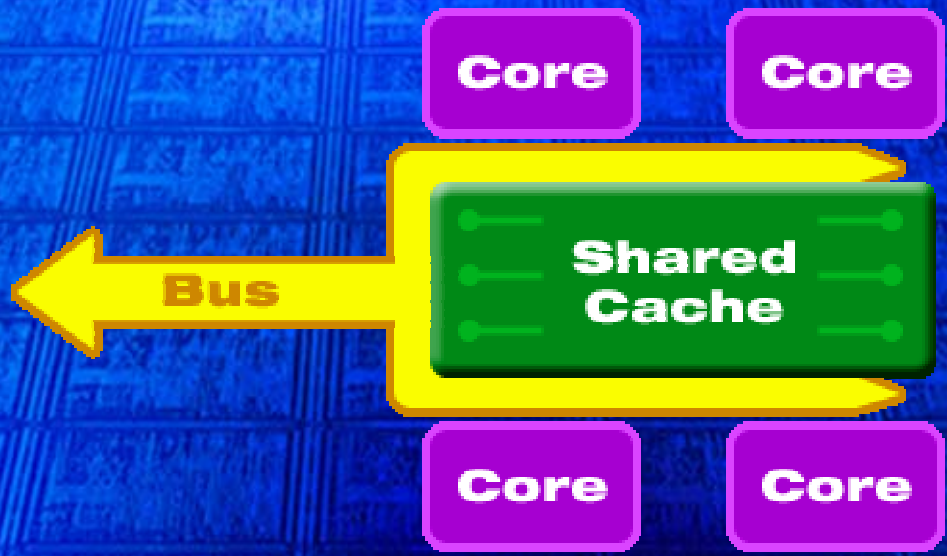
Power Management



- Enhanced Intel® SpeedStep™ Technology
  - Voltage-frequency scaling with active thermal feedback
  - Operating states range from high perf. to power efficient

Manage average and peak power dissipation

Multi-Core Enterprise Processor

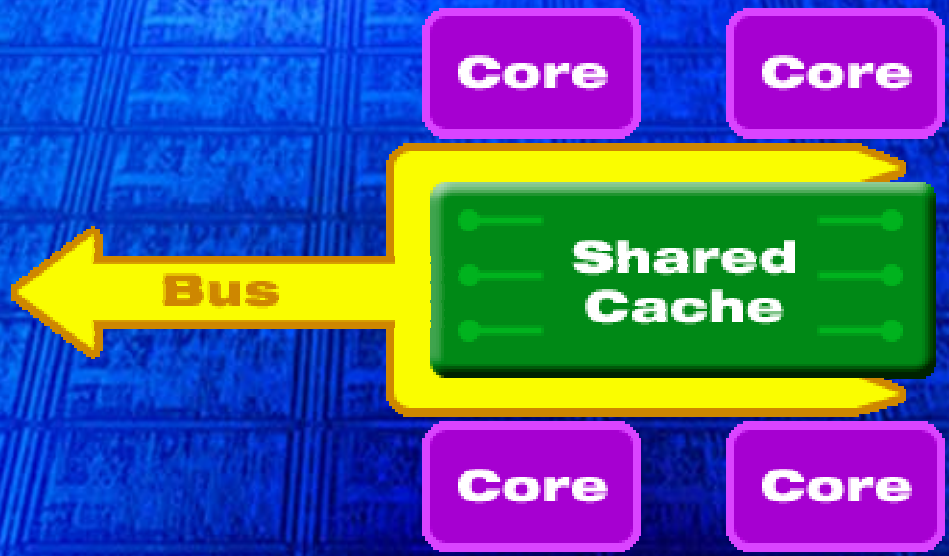


4 Processor system on a chip, Integrating:

- 4 Itanium 2 processor Cores ~120 M transistors
- Shared Cache 12-16 MB 700-950 M transistors
- Leaf interconnect

1B Transistors Can and Will be Used

Multi-Core Enterprise Processor



Power Addressed by:

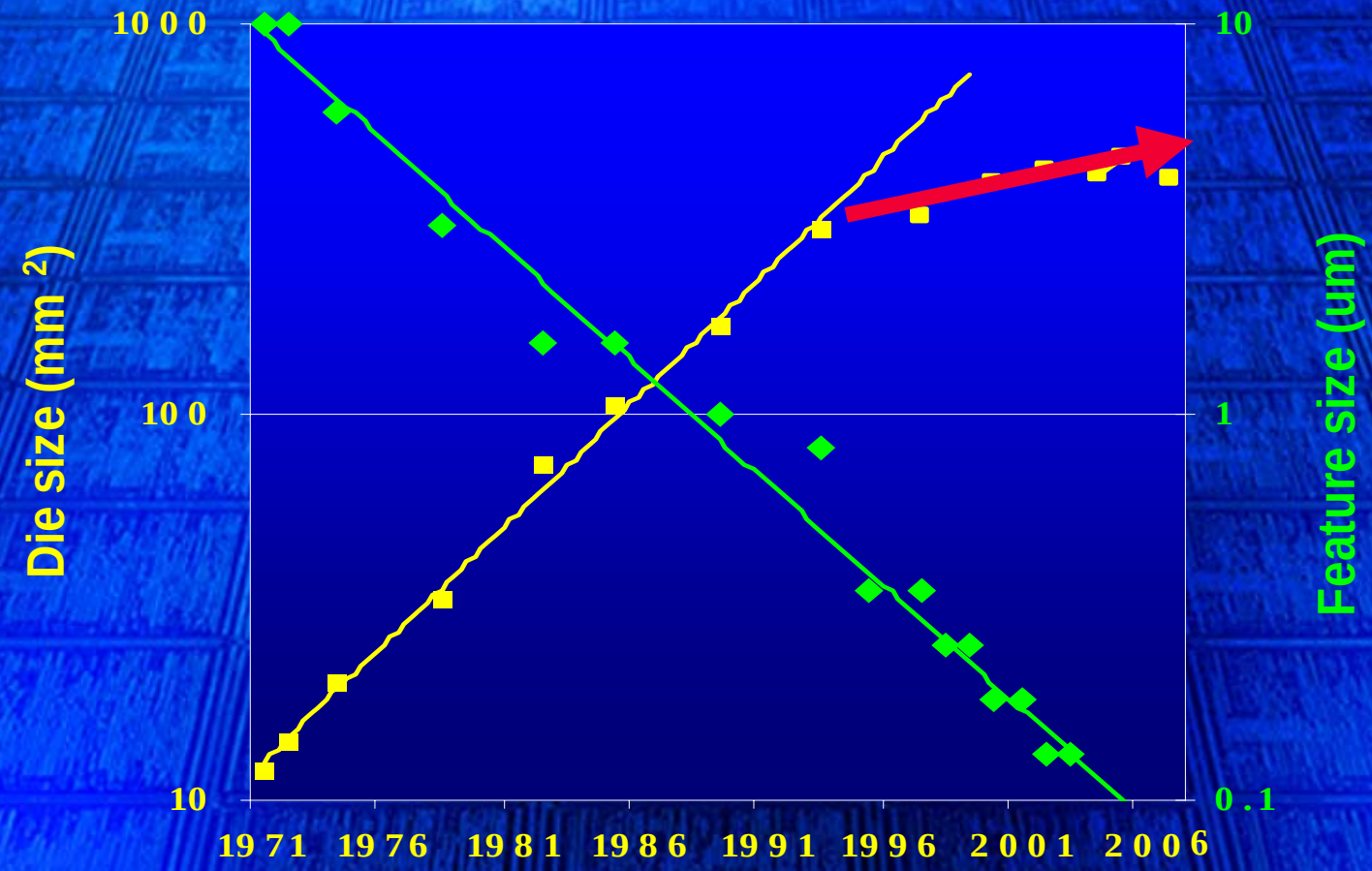
- Average out peaks among cores
- Spread hot spots in cores apart
- Cache has low power density
- Power Management techniques

Complexity Reduced by:

- Large Cache
- Repeat Cores

intel

Feature, Die Size Trend



Die size growth trend has moderated

1 Billion Transistors per CPU

- Continued Path of Moore's Law gets us to 1 Billion transistors around 2007
  - Reached 200 Million in 2002 with the Itanium® 2 Processor
- Performance structures will use 1B transistors
  - Example: Large cache, multi-threaded multi-core
    - Chip integration of today's board level integration
    - Complexity and power manageable; Addresses performance
- Design Challenges Grow as Transistors Shrink
  - Factory Cost, Test Visibility, Design Productivity, Power, …

Major innovations in both performance and beyond as the industry reaches 1 billion transistors

http://www.intel.com/pressroom/kits/events/mpf_2002/index.htm